

# Thermal stability of rare-earth based ultrathin Lu<sub>2</sub>O<sub>3</sub> for high-*k* dielectrics

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Lu<sub>2</sub>O<sub>3</sub> thin film was deposited on *n*-type (100) Si substrates using pulsed laser deposition. A *k* value of 15.95 with an equivalent oxide thickness (EOT) of 1.10 nm and a current density of  $2.6 \times 10^{-5}$  A/cm<sup>2</sup> at +1 V accumulation bias is achievable for the 4.5 nm thick Lu<sub>2</sub>O<sub>3</sub> thin film deposited at room temperature after postdeposition annealing at 600 °C in oxygen ambient. Annealing a similar sample at 900 °C caused the EOT and leakage current density to increase to 1.68 nm and  $1 \times 10^{-4}$  A/cm<sup>2</sup>, respectively. High resolution transmission electron microscopy analysis has shown that Lu<sub>2</sub>O<sub>3</sub> film remains amorphous at high temperature annealing at 900 °C. An x-ray reflectivity analysis on a separately prepared sample with lower annealing temperature (800 °C) suggested a formation of Lu-based silicate layer. It is believed that the formation of low-*k* silicate layer may have contributed to the observed increase in EOT and the reduction in the *k* value. © 2007 American Vacuum Society. [DOI: 10.1116/1.2749526]

## I. INTRODUCTION

The advancement of technology calls for complex applications, which requires the support of faster and more powerful electronic devices. The need for better performance devices has been met through the scaling of SiO<sub>2</sub> based devices. The use of SiO<sub>2</sub> as gate dielectric is fast reaching its fundamental limit to be an effective gate dielectric when the physical thickness is scaled down to below 1.5 nm due to the exponential increase of gate leakage current caused by quantum mechanical tunneling effect. This effect, if left unchecked, will cause a detrimental effect to the reliability of the device.<sup>1,2</sup>

Among the high-*k* gate dielectrics, ZrO<sub>2</sub> and HfO<sub>2</sub> have attracted much attention.<sup>3–6</sup> However, these materials still have some problems such as interfacial layer and microcrystal formations during the postdeposition annealing process. These problems lead to the increase of equivalent oxide thickness (EOT) and gate leakage current, respectively. In general, polycrystalline gate dielectrics may be problematic because grain boundaries serve as high-leakage paths. Moreover, grain size and orientation changes throughout a polycrystalline film can cause significant variation in the *k* value, leading to irreproducible properties.<sup>7</sup> In a transistor device, gate oxides must sit directly on Si, thus reaction, mixing, or interlayer formation during deposition are of primary concern. Also, in complementary metal oxide semiconductor (CMOS) processing, after gate oxide deposition, the transistor stack must be exposed to high temperature (>800 °C) (spike annealing or rapid thermal processing) to achieve the appropriate dopant profile in the transistor source and drain. Therefore, it is important to ensure that the gate dielectric oxide is thermally stable at high temperature. In this work,

we investigate the impact of high annealing temperature on Lu<sub>2</sub>O<sub>3</sub> thin film deposited using pulsed laser deposition (PLD).

The rare-earth oxides appear to be promising candidates as suitable replacements due to their advantageous properties such as fairly large band gap, high dielectric constant, and low leakage current,<sup>8–11</sup> which are required in order to be considered as suitable candidates to replace SiO<sub>2</sub> as high-*k* gate dielectric. Furthermore, some lanthanide oxides show good interfacial characteristics with little or no preformed interfacial layer.<sup>12</sup> In this work, Lu<sub>2</sub>O<sub>3</sub> is chosen as it has the highest lattice energy (–13 871 kJ/mol) and the largest band gap (5.5 eV),<sup>13–16</sup> from which we would expect Lu<sub>2</sub>O<sub>3</sub> to exhibit better thermal stability, good insulating property, and hygroscopic immunity as compared to other rare-earth oxide thin film. Lu<sub>2</sub>O<sub>3</sub> has been reported recently to exhibit good insulating properties with *k* value of around 11 as well as low gate leakage currents.<sup>17</sup> Other deposition methodology has been explored, such as high temperature oxidation of metallic films, ultrahigh vacuum electron-beam deposition,<sup>17</sup> and atomic layer deposition.<sup>18</sup> In our recent work,<sup>19</sup> the effect of N<sub>2</sub> and O<sub>2</sub> annealing ambients and the effect of light illumination on electrical behavior of Lu<sub>2</sub>O<sub>3</sub> were reported. A method to form nanodots embedded in Lu<sub>2</sub>O<sub>3</sub> using pulsed laser deposition for memory device application was also demonstrated.<sup>20,21</sup> In this work, we investigate the thermal stability in terms of material characteristics and its corresponding electrical properties of an ultrathin Lu<sub>2</sub>O<sub>3</sub> film as a function of annealing temperature and the corresponding influence on *I*-*V* and *C*-*V* measurements.

## II. EXPERIMENT

The Lu<sub>2</sub>O<sub>3</sub> thin films were deposited on *n*-type (100) Si using a Quasi-S customized pulsed laser deposition system

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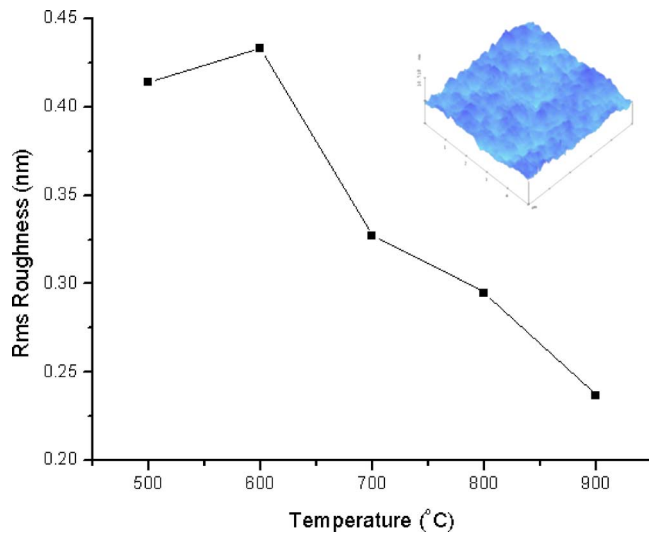


FIG. 1. rms roughness of Lu<sub>2</sub>O<sub>3</sub> film with the increment of annealing temperature. The inset shows relatively smooth surface with no observable microcrystallization for 900 °C annealing in oxygen ambient.

with a base vacuum of  $4.5 \times 10^{-7}$  Torr. The wavelength of the excimer laser is 248 nm and the energy density is  $1.8 \text{ J/cm}^2$  with the frequency set to 5 Hz. The substrates were first cleaned using Radio Corporation of America standard cleaning solution SC1, SC2 mixture, and then dipped in a 1% HF solution to remove the native oxide. The Lu<sub>2</sub>O<sub>3</sub> target for PLD was formed using ball milling for 24 h followed by high temperature sintering. In order to prevent the formation of SiO<sub>2</sub> interfacial layer during the thin film deposition, the Lu<sub>2</sub>O<sub>3</sub> films were deposited in high vacuum ( $4.5 \times 10^{-7}$  Torr) without introducing any oxygen gas. The thickness of the as-deposited Lu<sub>2</sub>O<sub>3</sub> thin films was about 4.5 nm. After deposition, these Lu<sub>2</sub>O<sub>3</sub> thin films were subjected to a postdeposition annealing (PDA) at temperatures ranging from 500 to 900 °C in oxygen ambient for 60 s. Top electrodes of Au with a diameter of 0.3 mm were sputtered for electrical measurement. Atomic force microscope (AFM) was used to examine the topology and smoothness of the films. The film thickness and interfacial property of sample annealed at 900 °C were examined using high resolution transmission electron microscope (HRTEM) with JEOL 2010 microscope and x-ray reflectivity (XRR) technique. For the XRR analysis, the films were investigated using high resolution x-ray specular reflectometry at grazing incidence angle with the Huber four-circle diffractometer, as described elsewhere.<sup>22</sup> The storage ring, Helios 2, was running at 700 MeV, typically stored electron-beam current of 300 mA. Diffuse scattering of rocking scan was also measured. Pure reflectivity was obtained by subtracting the diffuse scattering (background) from the raw data. The simulations were done using simulation software M805 and LEPTOS 1.07 release 2004 (Bruker). The electrical characteristics of the fabricated metal-insulator-semiconductor (MIS) devices, capacitance-voltage (*C-V*) was measured using a precision LCR meter (HP 4284A) at high frequency (100 kHz). The current den-

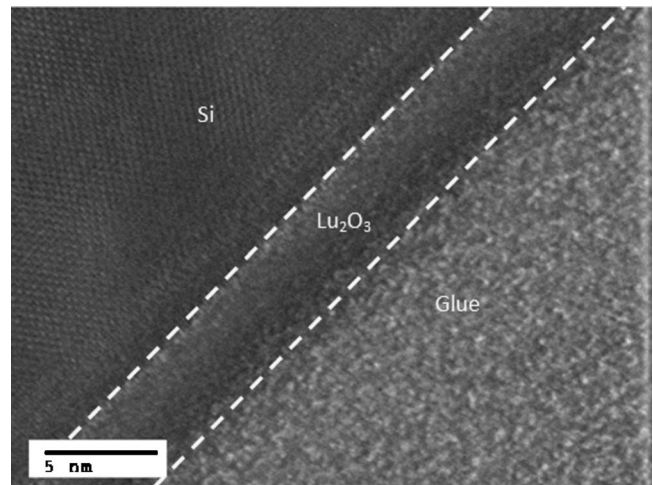


FIG. 2. Cross-sectional HRTEM image of Lu<sub>2</sub>O<sub>3</sub> films on *n*-type (100)Si revealing an amorphous structure with no observable interfacial layer for 900 °C annealing in oxygen ambient (Ref. 28).

sity versus voltage (*J-V*) was measured by a semiconductor parameter analyzer (Keithley 4200).

### III. RESULTS AND DISCUSSION

The root mean square (rms) roughness was obtained from the AFM analysis. A plot of rms roughness versus PDA temperature (Fig. 1) revealed a downward trend of decreasing roughness with increasing PDA temperature. The AFM images of various annealed samples did not show any evidence of crystallization. It is likely that the higher annealing temperature gives a higher thermal energy to the atoms which probably resulted in a more efficient migration of the deposited atoms and/or the enhancement of the densification of the films, which in turn gives a smoother surface of the film. The rms roughness of the 900 °C deposited film is 0.24 nm, this is comparable to a thermally grown SiO<sub>2</sub> film,<sup>23</sup> suggesting that the deposited film is smooth and uniform, without any distinct grain structure. There is no evidence of crystallization of the film from the AFM micrograph. This is further confirmed by the cross-sectional HRTEM image of the Lu<sub>2</sub>O<sub>3</sub> film on Si substrate after subsequent PDA at 900 °C, as shown in Fig. 2. It can be observed from the HRTEM micrographs that the Lu<sub>2</sub>O<sub>3</sub> thin film is relatively uniform and remains amorphous even after relatively high annealing step at 900 °C. Crystallization should be avoided for gate insulator application as it may cause an increase of the gate current through grain boundaries and/or fluctuation of device characteristics. The HTREM micrograph suggests that Lu<sub>2</sub>O<sub>3</sub> is thermally stable, at least up to 900 °C, which is close to the high temperature thermal annealing step for CMOS processing. An XRR analysis was performed on a sample which was annealed at 800 °C in N<sub>2</sub> ambient, in which the experimental and simulated curve is shown in Fig. 3. A two-layer model best fitted the experimental data indicating the presence of lutetium silicate formation at the interface. This result suggests that the silicate formation is likely to be caused by the presence of excess oxygen in Lu<sub>2</sub>O<sub>3</sub> that interacts

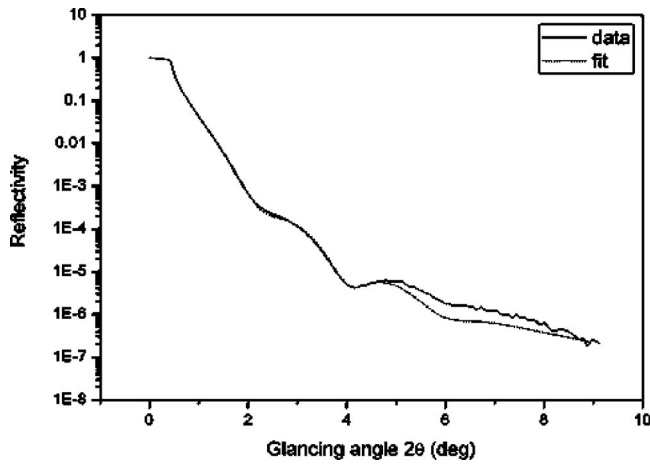


FIG. 3. XRR experimental and simulated data for  $\text{Lu}_2\text{O}_3$  thin film sample annealed at 800 °C.

with the Si substrate at an elevated temperature and/or indiffusion of (residual) oxygen from the annealing ambient. The growth of the silicate layer is currently being further investigated. The XRR analysis is summarized in Table I. The presence of the silicate layer is likely to have degraded the overall capacitance of the  $\text{Lu}_2\text{O}_3$  layer. This may in turn translate to lower  $k$  value and higher equivalent EOT of the overall gate stack structure.

The capacitance versus voltage characteristics of the MIS device ( $\text{Au}/\text{Lu}_2\text{O}_3/\text{Si}/\text{Au}$ ) annealed at 600 and 900 °C is shown in Fig. 4. The measurement was done at room temperature, using a high frequency of 100 kHz. A well shaped  $C$ - $V$  curve is obtained for both annealing temperatures, although degradation in the capacitance of the 600 °C annealed sample was observed. This degradation is likely to be caused by moisture absorption from the environment.<sup>17</sup> From the  $C$ - $V$  curve, the dielectric constant of the deposited  $\text{Lu}_2\text{O}_3$  was evaluated from the accumulation capacitance, without taking into account the quantum mechanical tunneling effect. The dielectric constants for the 600 and 900 °C annealed sample were evaluated to be 15.95 and 11.59, respectively. The EOT was determined by the relation proposed by Devoivre,<sup>24</sup> in which an EOT of 1.10 and 1.68 nm were obtained for the 600 and 900 °C annealed samples, respectively. The flatband voltage  $V_{\text{FB}}$  was estimated using the relation proposed by Motorola,<sup>25</sup> and we obtained a  $V_{\text{FB}}$  of -100 and -400 mV for the 600 and 900 °C annealed sample, respectively.

The 900 °C annealed sample appeared to have a lower  $k$  value and a higher EOT and  $V_{\text{FB}}$  as compared to the 600 °C

TABLE I. XRR simulation results for  $\text{Lu}_2\text{O}_3$  thin film sample annealed at 800 °C in  $\text{N}_2$  ambient.

Sample	Layers	Thickness (nm)	Roughness
800 °C anneal	$\text{Lu}_2\text{O}_3$	$2.2 \pm 0.1$	$0.65 \pm 0.08$
	$(\text{Lu}_2\text{O}_3)_x\text{Si}_y$ , interdiffused	$2.1 \pm 0.1$	$0.50 \pm 0.08$
	Si substrate		$0.1 \pm 0.1$

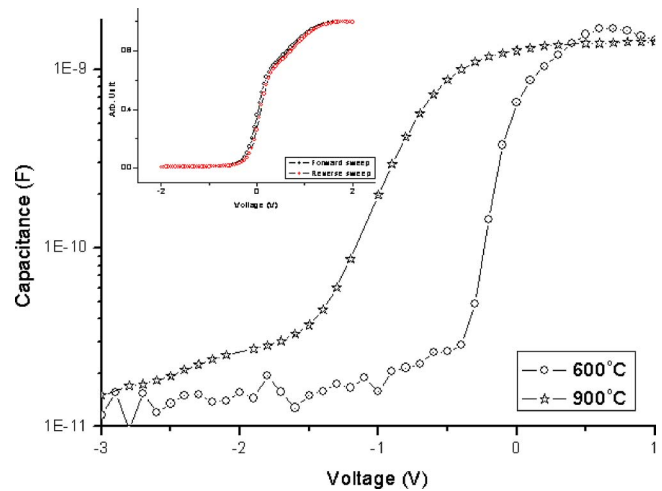


FIG. 4.  $C$ - $V$  characteristics of  $\sim 5$  nm  $\text{Lu}_2\text{O}_3$  film deposited on  $n$ -Si (100) substrate subjected to 900 °C RTA in oxygen ambient. The inset shows the hysteresis behavior of the  $\text{Lu}_2\text{O}_3$  film after 900 °C RTA in oxygen ambient.

annealed samples. One possible explanation is that the higher annealing temperature is likely to have caused some formation of a Si-Lu-O silicate layer, as observed in the XRR analysis for 800 °C annealed sample in nitrogen ambient, which may have a lower  $k$  value. This silicate layer is not obvious from the HRTEM image as a separate interfacial layer, but it is expected that the formation of a low- $k$  silicate will have an effect of lowering the overall capacitance value and increases the EOT of the film. This is reflected in our experimental data, in which the  $k$  value is lowered from 15.95 to 11.59 and the EOT increased from 1.10 to 1.68 nm.

The gold gate has an accepted work function of 5.31 eV.<sup>26</sup> The work function of  $n$ -type silicon with doping concentration of  $\sim 1 \times 10^{16} \text{ cm}^{-2}$  has a work function of 5.13 eV, which gives a work function difference of 0.18 eV. If there is no oxide charges present in the film, then the ideal flatband voltage ( $V_{\text{FB}}$ ) will be equal to the work function difference. Both samples have a negative  $V_{\text{FB}}$  which is indicative of positive fixed charges present in the film. The 900 °C has the larger shift away from the ideal value. This is likely to be caused by the higher defect present in the film related to the possible formation of the low- $k$  silicate layer. The presence of fixed charge in the gate dielectric should be avoided as it may have serious and deleterious effect on the device performance, especially in a transistor performance as the threshold voltage  $V_T$  may become too large for adequate compensation by dopant implants. The inset of Fig. 3 shows the hysteresis behavior of the 900 °C annealed sample. A small hysteresis of 50 mV is observed in the film, indicating the presence of some trapped charges in the film. The presence of trapped charges in the film, especially at the interface, should be kept small as it may reduce the drive current in metal oxide semiconductor field effect transistors as the trapped electron and holes act like charge scattering centers that lowers the mobility of the mobile carriers traveling in the surface channel. In addition, these interface states can also behave like localized generation-recombination centers

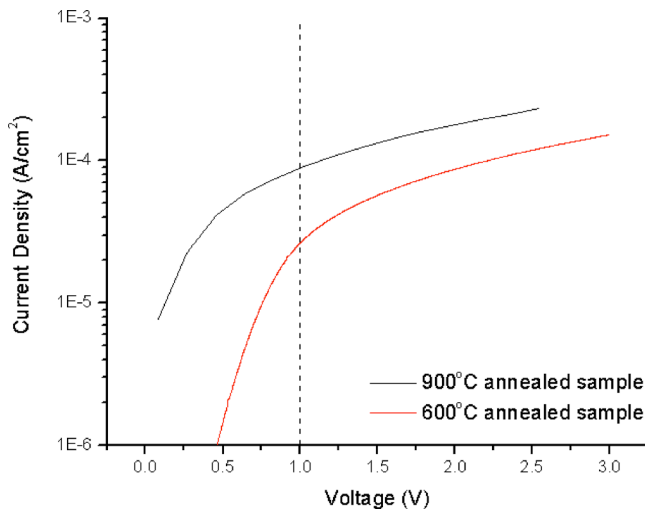


FIG. 5.  $J$ - $V$  characteristics of  $\sim 5$  nm Lu<sub>2</sub>O<sub>3</sub> film deposited on  $n$ -Si (100) substrate subjected to 900 and 600 °C RTA in oxygen ambient.

that can give rise to generation-recombination leakage currents and affecting the gate dielectric reliability.

Figure 5 shows the current density versus voltage ( $J$ - $V$ ) for the  $\sim 5$  nm thick Lu<sub>2</sub>O<sub>3</sub> film deposited at room temperature followed by an annealing step at 900 °C in oxygen ambient. The leakage current density at the off state of  $n$ -type Si substrate at +1 V bias was found to be  $1.0 \times 10^{-4}$  A/cm<sup>2</sup>. The low leakage current is several orders of magnitude lower than thermally grown SiO<sub>2</sub> with similar thickness. The low leakage current observed is attributed to the reduced oxygen vacancy as a result for the annealing step in oxygen ambient, thereby reducing the leakage current path.<sup>27</sup>

#### IV. CONCLUSIONS

In summary, Lu<sub>2</sub>O<sub>3</sub> thin films have been deposited on  $n$ -type (100) Si substrates using pulsed laser deposition. HR-TEM observation illustrated that the Lu<sub>2</sub>O<sub>3</sub> film has amorphous structure even after a high annealing temperature of 900 °C in oxygen ambient, although there is a likelihood that there is some formation of a lower- $k$  silicate layer (already observed for 800 °C annealed sample according to XRR analysis) which lowers the overall  $k$  value and increases the EOT. A well shaped  $C$ - $V$  characteristic was obtained and  $k$  values of 15.95 and 11.59 with EOTs of 1.10 and 1.68 nm was calculated for the 600 and 900 °C sample, respectively. The amorphous Lu<sub>2</sub>O<sub>3</sub> film annealed at 900 °C in oxygen ambient showed a low leakage current density of  $1.0 \times 10^{-4}$  A/cm<sup>2</sup> at +1 V bias for  $\sim 5$  nm thick Lu<sub>2</sub>O<sub>3</sub> thin film after the postannealing process in oxygen ambient. The results obtained have shown that Lu<sub>2</sub>O<sub>3</sub> has a good potential as a candidate to replace SiO<sub>2</sub> as a gate dielectric.

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