

Ge nanocrystals in lanthanide-based Lu₂O₃ high-*k* dielectric for nonvolatile memory applications

M. Y. Chan and P. S. Lee^{a)}

School of Materials Science and Engineering, Nanyang Technological University, Nanyang Avenue, Singapore 639798

V. Ho

Chartered Semiconductor Manufacturing Ltd., 60 Woodlands Ind. Park D, Street 2, Singapore 738406

H. L. Seng

Institute of Materials Research and Engineering (IMRE) 3, Research Link, Singapore 117602

(Received 10 July 2007; accepted 9 September 2007; published online 6 November 2007)

Ge nanocrystals embedded in lanthanide-based high-*k* dielectric (amorphous Lu₂O₃ in this work) were formed using pulsed laser deposition followed by rapid thermal annealing in N₂ ambient. The formation and evolution of the Ge nanocrystals have been studied using transmission electron microscopy (TEM), x-ray photoelectron spectroscopy (XPS) in conjunction with depth profiling, and secondary ion mass spectroscopy (SIMS) analysis. Plan-view TEM images indicated that the formation of nanocrystals was first initiated during the deposition process. The annealing treatment significantly enhanced the nucleation of Ge nanocrystals, resulting in a high areal density of $7 \times 10^{11} \text{ cm}^{-2}$ Ge nanocrystals with a mean size of about 6 nm in diameter in the amorphous Lu₂O₃ matrix. XPS depth profile analysis revealed that Ge nanocrystals were predominantly formed from the precipitation of Ge nuclei from the oxide phase. A low annealing temperature of 400 °C was sufficient to dissociate the GeO₂ and GeO_x leading to the formation of Ge nanocrystals. An accumulation of Ge species close to the upper Ge/Lu₂O₃ interface was observed from XPS and SIMS depth profile analysis. Different charge storage behaviors observed from the memory capacitor devices before and after annealing could be correlated to the changes in structure and composition of the film. The memory capacitor device fabricated from the annealed sample showed efficient charge storage effect under a low operation voltage without significant initial charge decay. © 2007 American Institute of Physics. [DOI: [10.1063/1.2803883](https://doi.org/10.1063/1.2803883)]

I. INTRODUCTION

Semiconductor nanocrystals embedded in a dielectric matrix have been extensively investigated due to their interesting physical phenomena and potential applications in optoelectronic and nanoelectronic devices. The utilization of nanocrystals as discrete charge storage nodes makes them more robust to stress-induced leakage current and allows for continuous scaling of flash memory device. Various nanocrystal synthesis methods have been intensively investigated, including cosputtering,^{1–3} ion implantation,^{4,5} chemical vapor deposition^{6,7} as well as oxidation of SiGe.^{8,9} More recently, the pulsed laser ablation technique has been studied as an attractive technique for the formation of nanocrystals with a narrow size distribution.^{10–13} Recent efforts have also focused on the utilization of high-*k* dielectrics in nanocrystal memory devices to achieve both good retention time and low voltage operation due to the unique band asymmetry in the programming and retention modes.¹⁴ Different high-*k* dielectric materials have been demonstrated for memory device applications, including HfO₂,^{14,15} ZrO₂,^{16,17} Al₂O₃,¹⁷ HfAlO,^{18,19} LaAlO₃,²⁰ and Lu₂O₃.¹⁰ In order to obtain a good quality high-*k* tunneling dielectric with a low density of interface traps, Lu₂O₃ was adopted due to its thermodynamical

stability and low leakage current characteristics, besides having a moderately high dielectric permittivity (~ 12).^{21–26} Furthermore, the utilization of Ge nanocrystals instead of Si nanocrystals as the floating gate material allows a greater potential for enhanced device performance due to the smaller band gap of Ge that provides both a higher confinement barrier for retention mode and a smaller barrier for program and erase mode.^{27–29} The demonstration of Ge nanocrystals in amorphous Lu₂O₃ high-*k* dielectric matrix for nonvolatile memory (NVM) device can be found in our previous work.¹⁰ In this work, the formation and evolution of Ge nanocrystals incorporated in Lu₂O₃ matrix were investigated based on transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS) analysis. Different charge storage mechanisms were proposed to explain the opposite hysteresis behavior that is strongly related to the composition and structure of the film before and after anneal. Efficient hole trapping events were observed from the annealed sample under low voltage operation, which makes it attractive for low voltage NVM applications.

II. EXPERIMENT

A KrF pulsed laser was used to ablate the target in an ultrahigh vacuum chamber. The wavelength of the excimer laser is 248 nm and the laser energy density is around

^{a)}Electronic mail: pslee@ntu.edu.sg

1.5 J/cm² with a frequency of 5 Hz. The pulsed laser deposition (PLD) target assembly has been illustrated in the previous work.¹⁰ *p*-type (100) Si substrates were first cleaned using SC1 and SC2 solutions, and then dipped into HF (1%) solution to remove the native oxide. The laser deposition was carried out in a high vacuum system (modified by Quasi-S Pte Ltd.) with a background pressure of about 6×10^{-7} Torr with the target rotating at about 30 rounds/min and the substrate was maintained at room temperature. During the PLD process, the target was kept stationary while allowing the laser to ablate the Lu₂O₃ for 2 min to form ~2 nm thick tunneling oxide layer. Subsequently, the target assembly was set to spin slowly about its central axis and the laser beam vaporized the two component materials alternately for 6 min to form ~6 nm of Ge nanocrystals embedded in Lu₂O₃ matrix. In order to prevent the degradation of electrical properties due to hygroscopic properties of Lu₂O₃, an additional Al₂O₃ capping layer was deposited by ablating a round Al₂O₃ (99.999%) target (diameter $D=25$ mm) for 3 min to form ~4 nm control oxide layer. With a high crystallization temperature and large band gap properties, Al₂O₃ could act as an effective blocking oxide due to an expected reduction in charge leakage to the control gate. After deposition, the film was subjected to postdeposition annealing (PDA) using rapid thermal processing (RTP) at 400 °C for 60 s in N₂ ambient.

The structural properties of the nanocrystals embedded in Lu₂O₃ matrix was examined using high-resolution transmission electron microscopy (HRTEM) with 200 kV accelerating voltage. XPS experiments were performed on the films without Al₂O₃ capping to study the chemical composition of the films before and after anneal. Photoelectron spectra were collected by means of a PHI 5600 XPS system using Al *K*α (energy=1486.6 eV) radiations at a take-off angle of 45°. In order to obtain the chemical composition as a function of depth from the as-deposited film, depth profiling was performed using Ar⁺ ions at an energy of 0.5 keV. In order to eliminate crater wall effects, the data were acquired from a smaller region ($300 \times 1400 \mu\text{m}^2$) in the center of the sputter area ($4 \times 4 \text{mm}^2$). Zalar rotation was used to minimize roughening of the samples due to ion bombardment. Secondary ion mass spectroscopy (SIMS) depth analysis was carried out to investigate the elemental distribution in the annealed film using a 1 keV Cs⁺ primary ion source.

Metal-insulator-semiconductor (MIS) memory capacitor structures were fabricated from the samples by evaporating Au top electrodes with 0.3 mm diameter and backside electrodes of ~500 nm thick after removing the native oxide on the wafer backside with 1% diluted HF. The memory behavior was investigated by performing capacitance-voltage (*C-V*) measurements at room temperature using HP4284A precision *LCR* meter. The programming characteristic was studied by electrically stressing the device at different voltages and subsequently monitoring the forward *C-V* sweep under a restricted bias sweep with a fast sweep rate to minimize charging up of the nanocrystals during the measurement. The charge retention behavior of the devices was studied by performing capacitance-time (*C-t*) measurements at room temperature.

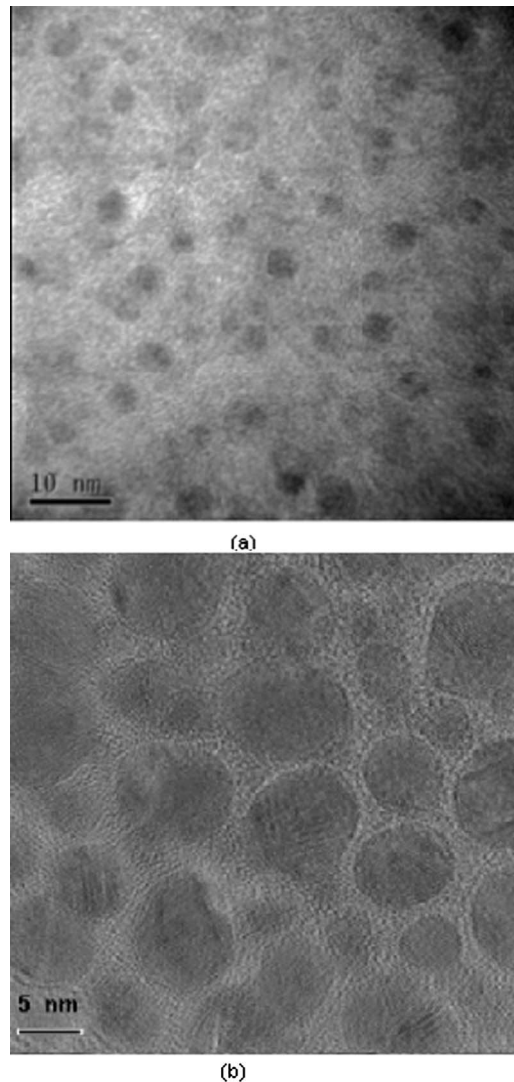


FIG. 1. (a) Planar TEM image of (a) as-deposited film and (b) 400 °C annealed film with Ge nanocrystals embedded in amorphous Lu₂O₃ dielectric matrix.

III. RESULTS AND DISCUSSION

Figure 1(a) shows the planar TEM image of the as-deposited film, with some dark contrast regions observed on the gray background, indicating the presence of nanoparticles in the oxide matrix. Small nanoparticles with 2–3 nm dimension and an areal density of $7 \times 10^9 \text{cm}^{-2}$ were observable from the image. The nanoparticle size is close to the estimated critical size for nucleation of Ge nanocrystals about 2 nm.²⁹ However, lattice fringes could not be clearly resolved in the dark areas, which could be related to the amorphous state or lattice instability in very small crystallites.²⁹ Figure 1(b) shows the planar TEM image of the film after PDA at 400 °C, with a large number of nanocrystals observed to precipitate densely in the amorphous Lu₂O₃ matrix. The annealing treatment resulted in an increased nanocrystal density of $7 \times 10^{11} \text{cm}^{-2}$ and larger crystallites with a mean size of 6 nm were obtained. The crystalline nature of the Ge dots is evidenced from the observed lattice planes with an interplanar distance of ~0.33 nm, which correspond to the (111) lattice planes of bulk Ge in the

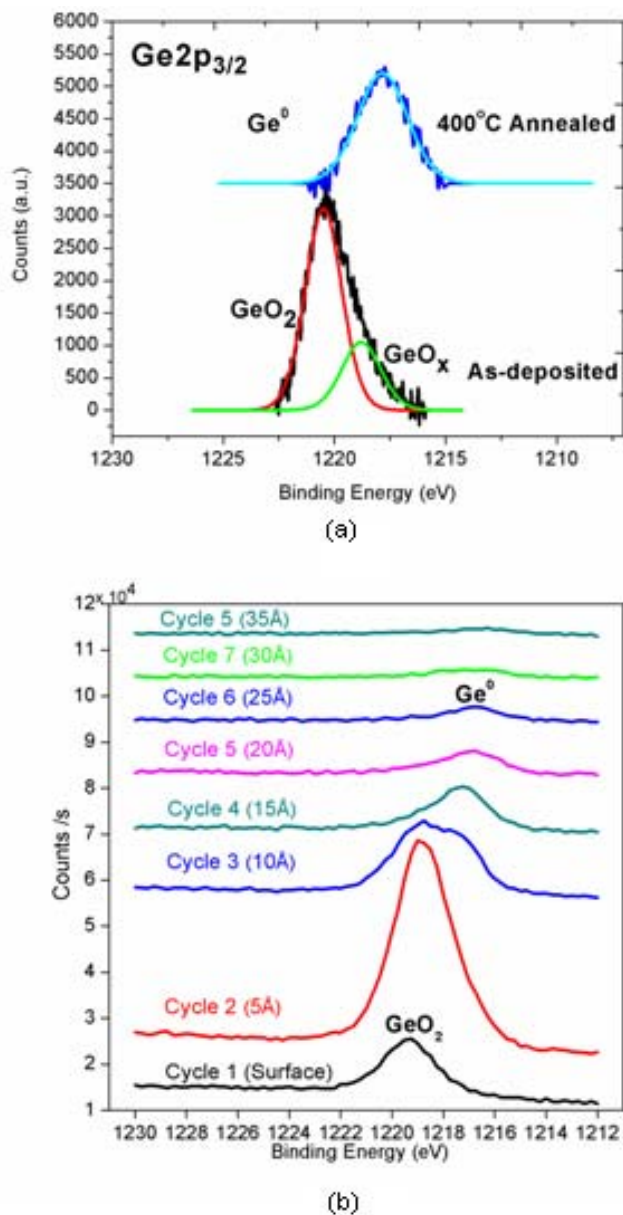


FIG. 2. (Color online) (a) Ge $2p_{3/2}$ core level XPS spectra of the film before and after N_2 anneal at $400\text{ }^\circ\text{C}$ and (b) Ge $2p_{3/2}$ stack plot with each spectrum obtained after each sputter cycle from the XPS depth profile measurement.

diamond cubic phase. Larger nanocrystals were observed indicating the growth and coalescence of smaller nanocrystals associated with the diffusion of Ge atoms during the annealing treatment. Besides that, twinning of the (111) planes was observed in some bigger crystalline dots larger than 5 nm. The simultaneous increase in nanocrystal size and density achieved after annealing is favorable to ensure sufficient amount of charge storage for detectable threshold voltage shift of the memory device.³⁰ At the same time, sufficient intercrystallite separation is maintained to obtain electrically isolated storage nodes.

The chemical composition of the films with and without PDA was revealed by XPS depth profile analysis. As shown in Fig. 2(a), the Ge $2p_{3/2}$ XPS spectra of the as-deposited sample indicates the existence of Ge in its oxidized state,

with a fitted main peak at higher binding energy corresponding to GeO_2 (1220.5 eV) and a small lower binding energy peak to GeO_x (1218.8 eV). After the annealing treatment at $400\text{ }^\circ\text{C}$, the $Ge2p_{3/2}$ peak shifted down to 1217.7 eV, corresponding to the existence of Ge in the elemental state. The results suggest that Ge–O bonds were created during codeposition with Lu_2O_3 , which is similar to the observations from the films deposited by cosputtering with the incorporation of Ge oxides.^{29–32} In Fig. 2(b), the XPS depth profile for Ge provides information on the chemical state of Ge throughout the as-deposited film. It was found that the film consists of a subsurface region with Ge existing in the oxide phase (GeO_2 and GeO_x), and the existence of elemental Ge phase was revealed in the bulk, after a few sputter cycles. However, Ge exists predominantly in the oxide phase throughout the film, with only a low concentration of elemental Ge present at larger depth, as observed from the significantly lower integrated intensity of the Ge^0 peak compared to the GeO_2 and GeO_x peaks. The small amount of elemental Ge initially contained in the matrix can provide nuclei for the formation of nanocrystals, if the size is sufficiently larger than the critical size.²⁹ This suggests likely the nucleation of very small Ge precipitates possibly close to the critical nuclei size in the initial deposit, which is in good agreement with the presence of small nanoparticle regions observed from the planar TEM image in Fig. 1(a). However, a large fraction of Ge was oxidized during the deposition process and exists as Ge oxide in Lu_2O_3 matrix.

Based on the structural and compositional analyses, the nanocrystal formation process could be described from the thermodynamics point of view. The as-deposited film could be considered as a supersaturated solution containing a large amount of excess Ge oxides and a small amount of elemental state Ge. The high kinetic energy of plasma generated during the laser ablation process resulted in an enhanced adatom mobility during the deposition process, and some small crystallites could be formed from the preexisting Ge atoms when the diffusing Ge atoms bond to existing nuclei. During the annealing treatment, a spontaneous reduction reaction of Ge oxides and suboxides occurred, leading to the creation of a large amount of elemental Ge atoms. Hence the process of nanocrystal formation primarily took place with the precipitation of Ge nuclei corresponding to the reduction of Ge oxides upon annealing. This is evidenced from the densely distributed Ge nanocrystals observed from the plan-view TEM image of the annealed film, indicating a significant increased nucleation of Ge nanocrystals associated with the reduction process during the annealing treatment. The simultaneous increase in the average size and size distribution of the nanocrystals after annealing can be explained by the growth and aggregation of the Ge precipitates initially contained in the matrix. The final size of the nanocrystals are determined by the nucleation of Ge from the reduction of GeO_2 , as well as subsequent growth and coarsening process via the Ostwald ripening mechanism,^{29,33} whereby larger particles grow at the expense of smaller particles.

The dissociation of GeO_2 and GeO_x under a low annealing temperature of $400\text{ }^\circ\text{C}$ can be explained from the thermodynamics perspectives, whereby a large negative Gibbs

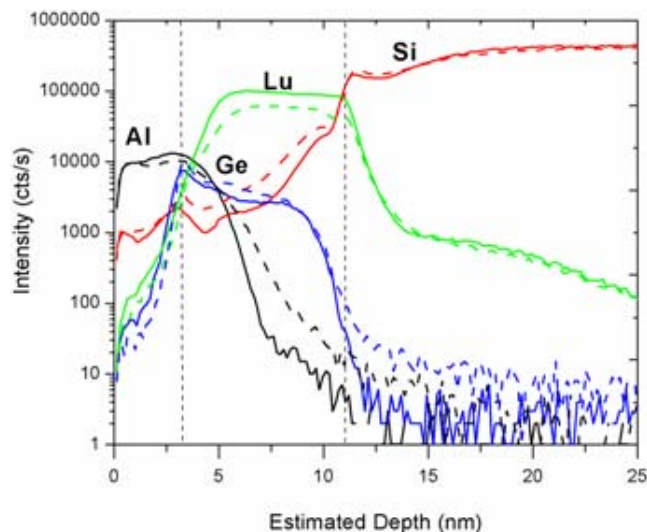


FIG. 3. (Color online) (a) SIMS depth profiles of Al, Si, Ge, and Lu measured as a function of depth into the Si substrate, with the solid lines plotted for the as-deposited film and dashed lines plotted for the 400 °C annealed film.

free energy change (ΔG) involved provides a highly energetically favorable reaction to proceed rapidly. A possible reducing species involved in the dissociation process is from the small amount of substoichiometric Lu oxides existing in the oxide matrix due to oxygen deficiencies. Due to the contribution of the significantly larger Gibbs free energy of formation ($\Delta_f G^0 = -1789.0 \text{ kJ mol}^{-1}$) for Lu_2O_3 (Ref. 34) as compared to other oxides, a large driving force could be provided for the substoichiometric Lu_2O_3 to react with Ge oxides, leading to the formation of stoichiometric Lu_2O_3 and Ge. This could be related to the significant reduction observed under a low annealing temperature, which is different from the previously reported works that require a high temperature anneal above 600 °C for the observations of reduction reaction.^{35–38} However, the small chemical shift (0.1 eV) exhibited by the Lu atom resulted in difficulties in determining different oxidation states present in the matrix. The relative atomic concentration of each element was quantified by integrating each peak, and the O/Lu ratio of ~ 1.33 obtained from the as-deposited film indicates a small degree of nonstoichiometry due to oxygen deficit in the dielectric matrix, which could act as the source for the reduction reaction.

Figure 3 shows the SIMS depth profile of each element in the direction from the film surface to the Si substrate for the as-deposited and 400 °C annealed sample. Minimal differences were observed from the profiles after annealing, except for some slight difference in the slope of the falling edge for the Al and Ge profiles. However, the in-diffusion of Al and Ge atoms could not be determined based on the small changes in the slope profiles as tailing effects due to ion bombardment were expected to occur during the sputtering process. Nevertheless, the Ge atoms were well-distributed within the middle region of $\sim 6.5 \text{ nm}$ thick before and after anneal, which is in good agreement with the expected distribution. Besides that, both Ge profiles show the appearance of a small peak near the interface with the Al_2O_3 control dielec-

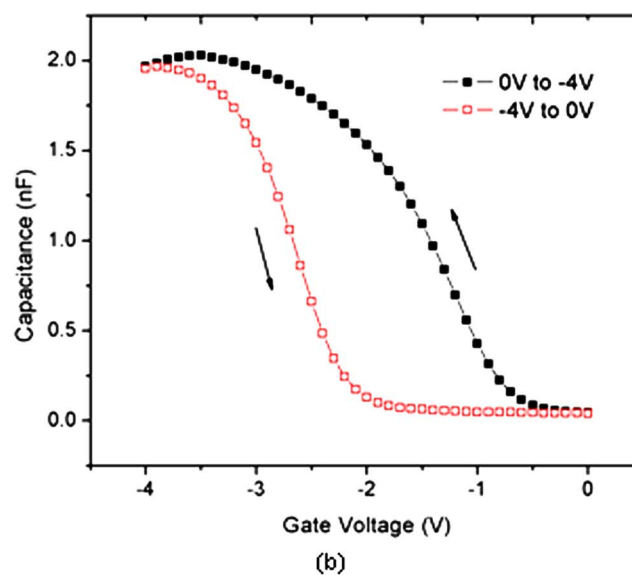
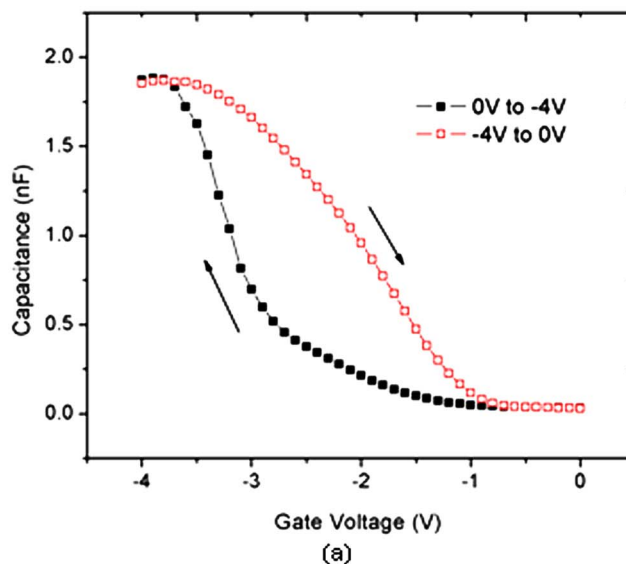


FIG. 4. (Color online) (a) High-frequency (100 kHz) capacitance-voltage characteristics of the MIS devices (a) without and (b) with PDA at 400 °C.

tric, suggesting a pile up of Ge atoms in the vicinity of the upper interface during the deposition process.

Figure 4 shows the high-frequency (100 kHz) C - V hysteresis loops of the MIS devices obtained by applying bidirectional gate voltage sweep between 0 and -4 V . An opposite hysteresis behavior was observed between the devices with and without PDA, which suggests the involvement of different mechanisms in the charge trapping process. The anticlockwise hysteresis loop observed from the annealed device is generally attributed to the charge storage of the nanocrystals via substrate injection mechanism. When a positive voltage is applied to the gate, electrons can tunnel from the deep inversion layer of the substrate to the nanocrystals via substrate injection mechanism.^{39–41} When a negative voltage is applied to the gate, electrons can tunnel from the nanocrystals (and/or holes can tunnel from the deep accumulation layer of the substrate to the nanocrystals), resulting in a shift of the C - V curve towards negative voltages.³⁹ A significant

charge storage effect was demonstrated in Fig. 4(b) with a large flatband voltage shift of ~ 1.3 V obtained from the annealed device. The number of trapped charges was estimated to be $7.0 \times 10^{12} \text{ cm}^{-2}$ from the flatband voltage shift obtained, which gives an estimation of ten charges stored in a nanocrystal. The large stored charge density is attributed to the presence of localized traps at the interface between the nanocrystals and the oxide or at the internal traps of the nanocrystals.^{42–46} Since no distortion, e.g., flat step due to deep defect traps or large interface state density, was observed⁴⁷ in the C - V curves, the hysteresis effect is likely related to the charging of the Ge nanocrystals or nanocrystal-related traps. On the other hand, the clockwise hysteresis from the device without PDA in Fig. 4(a) could be associated to different compositional and structural properties of the film before anneal. Based on the XPS analysis, it can be deduced that the as-deposited film consists of a Ge-rich mixture with a large fraction of Ge oxides and a small amount of Ge precipitates. Hence a substantial amount of interface traps and structural defects, e.g., weakly bonded GeO_x , were created, which resulted in mixed charge trapping effects at the interface and defect states. With the larger amount of interface states and defects existing in the oxide before annealing, it is plausible to assume that defect-related charging dominates, whereby charges were transferred between the traps at the excess Ge and Ge oxides as well as surrounding oxide defects or trapped at the interface and defect states in the oxide matrix.⁴⁸ Hence the large density of oxide defects prevents effective charge injection from the substrate, resulting in a reverse hysteresis behavior. This is apparent from the stretch-out in the C - V curve observed when the gate voltage was swept from inversion into the depletion region, indicating the contribution of interface traps in the C - V characteristics.

Figure 5(a) shows the programming characteristics of the annealed device before and after charging with sequentially increasing programming voltages, with a holding time of 10 s for each programming voltage. The initial C - V curve obtained before performing the charging measurements can be treated as the quasineutral condition (i.e., the uncharged condition) under a restricted bias sweep. A negligible shifting of the curves was obtained under a positive applied bias, while the C - V curves consistently shifted towards more negative gate voltages with increasing negative programming voltages as a larger amount of holes were trapped in the nanocrystals. This indicates that the major charge storage of the memory device is due to hole contribution, with negligible electron charging effect observed. Figure 5(b) shows the magnitude of the shift in flatband voltage V_{FB} with respect to the quasineutral condition (ΔV_{FB}) plotted as a function of the applied programming voltage. It is shown that a significant V_{FB} shift of 0.52 V was already obtained under a low programming voltage of -2 V, and the V_{FB} shift progressively increased with increasing programming voltages. A maximum V_{FB} shift of 1.32 V was obtained for programming voltages of -4 V and beyond, corresponding to the saturation of charge storage. Hence an effective hole trapping phenomenon demonstrated with a large V_{FB} shift obtained under low operation voltages.

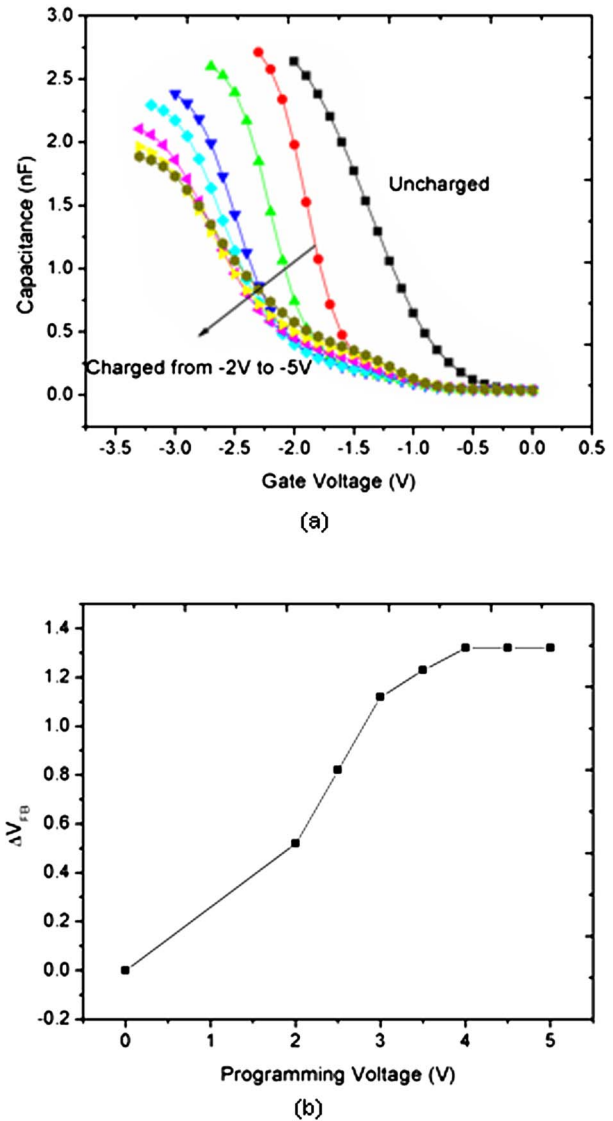


FIG. 5. (Color online) (a) C - V characteristics of the memory capacitor device obtained before and after applying sequential negative programming voltages with a stress time of 10 s and (b) the corresponding flatband voltage shift as a function of programming voltages.

Figure 6 shows the charge retention characteristics of the annealed memory capacitor, with the normalized capacitance plotted as a function of discharging time. After charging the device under an applied bias of -3 V for 10 s, the capacitance was monitored as a function of time under the flatband condition of the device at -1 V. The onset of the discharging process was only observed after a holding time of 100 s with no significant initial fast decay characteristic observed. 5% of the initial stored charge was lost after a holding time of 1000 s, maintaining a sufficient memory window to be easily current-sensed. As no significant charge storage loss was found up to 1000 s, a good stability of the programmed state is expected from the observed charge decay behavior. The long term charge storage characteristic of the device is also shown in Fig. 6 (inset). A gradual decrease of memory effect was observed, with a measured retention time of 10^4 s for 25% charge storage loss obtained, which is satisfactory as compared to devices with similar equivalent oxide thickness (EOT).^{49,50}

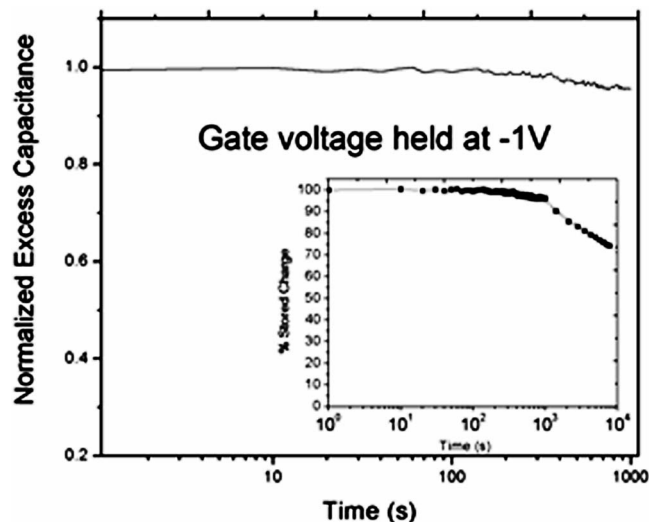


FIG. 6. Normalized charge decay characteristics of the annealed memory capacitor device after charging at -3 V for 10 s.

IV. CONCLUSION

In summary, this work presents the promising potential of the memory structure with Ge nanocrystals embedded in lanthanide-based Lu_2O_3 high- k dielectrics for low voltage NVM applications. The nanocrystal formation process was described based on the thermodynamics contribution through the reduction of Ge oxides and suboxides during the annealing process, leading to the nucleation and subsequent growth of Ge nanocrystals. A low annealing temperature of 400°C is sufficient for the spontaneous reduction reaction and formation of Ge nanocrystals. The results also outline the significant role of annealing on the improvement of charge storage behavior, which could be correlated to the formation of Ge nanocrystals corresponding to the reduction of Ge oxides and a simultaneous improvement in the oxide film quality upon annealing. This allows a significant charge storage capability achieved under low operation voltage, with sufficient retention maintained from the annealed device.

ACKNOWLEDGMENTS

This work is financed in part by A*Star SERC No. 042 114 0050. One of the authors (M.Y.C.) is grateful for the research scholarship provided by School of Materials Science and Engineering in Nanyang Technological University and Chartered Semiconductor Manufacturing Singapore.

- ¹M. Fujii, S. Hayashi, and K. Yamamoto, *Jpn. J. Appl. Phys., Part 1* **30**, 687 (1991).
- ²V. Ho, L. W. Teo, W. K. Choi, W. K. Chim, M. S. Tay, D. A. Antoniadis, E. A. Fitzgerald, A. Y. Du, C. H. Tung, R. Liu, and A. T. S. Wee, *Appl. Phys. Lett.* **83**, 3558 (2003).
- ³Y. Q. Wang, J. H. Chen, W. J. Yoo, Y. C. Yeo, S. J. Kim, R. Gupta, Z. Y. L. Tan, D. L. Kwong, A. Y. Du, and N. Balasubramanian, *Appl. Phys. Lett.* **84**, 5407 (2004).
- ⁴S. K. Min, K. V. Shcheglov, C. M. Yang, H. Atwater, M. L. Brogersman, and A. Polman, *Appl. Phys. Lett.* **68**, 2511 (1996).
- ⁵N. Kishimoto, Y. Takeda, V. T. Gritsyna, E. Iwamoto, and T. Saito, *Proceedings of Ion Implantation Technology* (IEEE, Piscataway, New Jersey, 1999).
- ⁶J. H. Shin, H. S. Han, S. Y. Seo, and W. H. Lee, *J. Korean Phys. Soc.* **34**, s16 (1999).
- ⁷S. Lombardo, S. Coffa, C. Bongiorno, C. Spinella, E. Castagna, S. Sciuto,

- C. Gerardi, F. Ferrari, B. Frazio, and S. Privitera, *Mater. Sci. Eng., B* **69**, 295 (2000).
- ⁸Y. C. King, T. J. King, and C. Hu, *IEEE Trans. Electron Devices* **48**, 696 (2001).
- ⁹T. Sass, V. Zela, A. Gustafsson, I. Pietzonka, and W. Seifert, *Appl. Phys. Lett.* **81**, 3455 (2002).
- ¹⁰C. L. Yuan, P. Darmawan, Y. Setiawan, and P. S. Lee, *Europhys. Lett.* **74**, 177 (2006).
- ¹¹C. L. Yuan, P. Darmawan, Y. Setiawan, P. S. Lee, and J. Ma, *Appl. Phys. Lett.* **89**, 043104 (2006).
- ¹²W. L. Liu, P. F. Lee, J. Y. Dai, J. Wang, H. L. W. Chan, C. L. Choy, Z. T. Song, and S. L. Feng, *Appl. Phys. Lett.* **86**, 013110 (2005).
- ¹³K. M. Hassan, A. K. Sharma, J. Narayan, J. F. Muth, C. W. Teng, and R. M. Kolbase, *Appl. Phys. Lett.* **75**, 1222 (1999).
- ¹⁴J. J. Lee, X. Wang, W. Bai, N. Lu, and D. L. Kwong, *Symp. VLSI Tech. Dig.*, **33** (2003).
- ¹⁵D. W. Kim, T. Kim, and S. K. Banerjee, *IEEE Trans. Electron Devices* **50**, 1823 (2003).
- ¹⁶D. W. Kim, F. E. Prins, T. Kim, S. Hwang, C. H. Lee, D. L. Kwong, and S. K. Banerjee, *IEEE Trans. Electron Devices* **50**, 510 (2003).
- ¹⁷Q. Wan, N. L. Zhang, W. L. Liu, C. L. Lin, and T. H. Wang, *Appl. Phys. Lett.* **83**, 138 (2003).
- ¹⁸P. F. Lee, X. B. Lu, J. Y. Dai, H. L. W. Chan, E. Jelenkovic, and K. Y. Tong, *Nanotechnology* **17**, 1202 (2006).
- ¹⁹Y. Q. Wang, J. H. Chen, W. J. Yoo, Y. C. Yeo, S. J. Lim, D. L. Kwong, A. Y. Du, and N. Balasubramanian, *Appl. Phys. Lett.* **84**, 5407 (2004).
- ²⁰X. B. Lu, P. F. Lee, and J. Y. Dai, *Appl. Phys. Lett.* **86**, 203111 (2005).
- ²¹G. Scarel, E. Bonera, C. Wiemer, G. Tallarida, S. Spiga, and M. Fanciulli, *Appl. Phys. Lett.* **85**, 630 (2004).
- ²²S. Ohmi, M. Takeda, H. Ishiwara, and H. Iwai, *J. Electrochem. Soc.* **151**, G279 (2004).
- ²³D. G. Schlom and J. H. Haeni, *MRS Bull.* **27**, 198 (2002).
- ²⁴L. Marsella and V. Fiorentini, *Phys. Rev. B* **69**, 172103 (2004).
- ²⁵G. Lucovsky, Y. Zhang, G. B. Rayner, G. Appel, and H. Ade, *J. Vac. Sci. Technol. B* **20**, 1739 (2003).
- ²⁶P. Darmawan, C. L. Yuan, and P. S. Lee, *Solid State Commun.* **138**, 571 (2006).
- ²⁷O. Winkler, F. Merget, M. Heuser, B. Hadam, M. Baus, B. Spangenberg, and H. Kurz, *Microelectron. Eng.* **61**, 497 (2002).
- ²⁸T. Usuki, T. Futatsugi, and N. Yokoyama, *Microelectron. Eng.* **47**, 281 (1999).
- ²⁹Y. Maeda, *Phys. Rev. B* **51**, 1658 (1995).
- ³⁰H. I. Hanafi, S. Tiwari, and I. Khan, *IEEE Trans. Electron Devices* **43**, 1553 (1996).
- ³¹H. Fukuda, T. Kobayashi, T. Endoh, and Y. Ueda, *Appl. Surf. Sci.* **130–132**, 776 (1998).
- ³²W. K. Choi, V. Ho, V. Ng, Y. W. Ho, S. P. Ng, and W. K. Chim, *Appl. Phys. Lett.* **86**, 143114 (2005).
- ³³S. Oswald, B. Schmidt, and K. Heinig, *Surf. Interface Anal.* **29**, 249 (2000).
- ³⁴*CRC Handbook of Chemistry and Physics*, 84th ed., edited by D. R. Lide (CRC, Boca Raton, 2003).
- ³⁵F. Zheng, H. G. Chew, W. K. Choi, J. X. Zhang, and H. L. Seng, *J. Appl. Phys.* **101**, 114310 (2007).
- ³⁶Y. Q. Wan, J. H. Chen, W. J. Yoo, Y. C. Yeo, S. J. Lim, D. L. Kwong, A. Y. Du, and N. Balasubramanian, *Appl. Phys. Lett.* **84**, 5407 (2004).
- ³⁷A. K. Dutta, *Appl. Phys. Lett.* **68**, 1189 (1996).
- ³⁸D. C. Paine, C. Caragianins, T. Y. Kim, T. Shigesato, and T. Ishikawa, *Appl. Phys. Lett.* **62**, 2842 (1993).
- ³⁹Ch. Sargentis, K. Giannakopoulos, A. Travlos, N. Boukos, and D. Tsamakis, *Appl. Phys. Lett.* **88**, 073106 (2006).
- ⁴⁰Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, *J. Appl. Phys.* **84**, 2358 (1998).
- ⁴¹A. Kanjilal, L. Lundsgaard Hunsen, P. Gaiduk, A. Nylandsted Larsen, N. Cherkashin, A. Clavierie, P. Normand, E. Kapelanakis, D. Dkarlatos, and D. Tsoukalas, *Appl. Phys. Lett.* **82**, 1212 (2003).
- ⁴²D. N. Kouvatso, V. Ionno-Sougleridis, and A. G. Nassiopoulou, *Appl. Phys. Lett.* **82**, 397 (2003).
- ⁴³S. J. Baik, S. Choi, U.-I. Chung, and J. T. Moon, *Solid-State Electron.* **48**, 1475 (2004).
- ⁴⁴Y. H. Kwon, C. J. Park, W. C. Lee, D. J. Fu, Y. Shon, T. W. Kang, C. Y. Hong, H. Y. Cho, and K. L. Wang, *Appl. Phys. Lett.* **80**, 2502 (2002).
- ⁴⁵E. Kapetankis, P. Normand, D. Tsoukalas, K. Beltsios, J. Stoemenos, S.

Zhang, and J. van den Berg, Appl. Phys. Lett. **77**, 3450 (2000).

⁴⁶M. She and T. J. King, IEEE Trans. Electron Devices **50**, 1934 (2003).

⁴⁷B. Liss and O. Engstrom, J. Appl. Phys. **78**, 1824 (2005).

⁴⁸J. Y. Tseng, C. W. Cheng, S. Y. Wang, T. B. Wu, K. Y. Tsieh, and R. Liu,

Appl. Phys. Lett. **85**, 2595 (2004).

⁴⁹T. Baron, A. Fernandes, J. F. Damlencourt, B. De Salvo, F. Martin, and F. Mazen, Appl. Phys. Lett. **82**, 4151 (2003).

⁵⁰M. Saitoh, E. Nagata, and T. Hiramoto, IEDM Tech. Dig., **181** (2002).